

PCB Production Specification

Antenna Processing Subrack Clock and Translator (APSCT)

PCB nr.: 03116

	Organisatie / Organization	Datum / Date
Auteur(s) / Author(s): Gijs Schoonderbeek Sieds Damstra	ASTRON ASTRON	11-03-2021
Controle / Checked: Nico Ebbendorf	ASTRON	
Goedkeuring / Approval: Gijs Schoonderbeek	ASTRON	
Autorisatie / Authorisation: Handtekening / Signature	ASTRON	
© ASTRON All rights are reserved. Reproduction in whole or in part is prohibited without written consent of the copyright owner.		



This publication is part of the project DUPLLO (with project number 175.2017.012 of the research program "Investerings NWO-groot" which is (partly) financed by the Dutch Research Council (NWO).

Doc.nr.: PSF00167
Rev: 3.0
Date: 11-03-2022
Class.:

Distribution list:

Group:	Others:
Gijs Schoonderbeek Sieds Damstra	N. Ebbendorf A. v. Duin H. Meulman

Document history:

Revision	Date	Chapter / Page	Modification / Change
0.1	15-03-2021	-	Creation
0.2	18-03-2021	-	
1.0	15-04-2021	-	Update for production
1.1	31-05-2021	-	Remarks PCB Manf.
2.0	05-01-2022		Update for tender version.
3.0	11-03-2022		Update after review

Table of contents:

Distribution list:	2
1 Introduction	3
1.1 Document Scope	3
1.2 Applicable documents (AD)	3
1.3 Reference documents (RD)	3
1.4 List of Terms and acronyms	3
2 IPC Quality Requirements	3
2.1 Board:	Error! Bookmark not defined.
3 Specifications	4
4 List of Files	5
Manufacture notes	6



This publication is part of the project DUPLLO (with project number 175.2017.012 of the research program "Investeren in NWO-groot" which is (partly) financed by the Dutch Research Council (NWO).

PSF00167
3.0
11-03-2022

1 Introduction

1.1 Document Scope

This document presents technical PCB production specification for the APSCT, Clock and Translator board for Antenna Processing Subrack for LOFAR 2.0. For all specification is the **ODB++ DATA IS LEADING**

1.2 Applicable documents (AD)

Ref.nr.	Document number	Rev.	Title	File name
AD.1	PPD00064	0.1	PCB Production data APSCT (ODB++ file)	apsct_180222.tgz

1.3 Reference documents (RD)

Ref.nr.	Document number	Title	Author
RD.1	PMS00044	PMS APSCT	

1.4 List of Terms and acronyms

BOM	Bill Of Material
IPC	Association Connecting Electronics Industries
PCB	Printed Circuit Board

2 IPC Quality Requirements

The board have the following IPC requirements:

IPC requirement	Comment
IPC 2222B	Board type 3 (Multilayer Printed Board without blind and/or buried vias)
IPC 2221A	Performance Class 2 (Dedicated Service Electronic Products). Producibility Level B (High Design Complexity - Standard)
IPC A-600	Class 2 (Dedicated Service Electronic Products)
IPC SM-840	Solder Resist
IPC 4101	Laminate Material



This publication is part of the project DUPLLO (with project number 175.2017.012 of the research program "Investeringen NWO-groot" which is (partly) financed by the Dutch Research Council (NWO).

PSF00167
3.0
11-03-2022

Bare board testing

- Impedances on all impedance layer shall be tested according IPC-TM-650 2.5.5.7. Both single ended and differential impedance will be <10% with the specified impedance. A report showing compliance shall be delivered with the board or send to schoonderbeek@astron.nl

Remarks

PCB supplier should send ASTRON the test results after board testing.

3 Specifications

PCB nr.	03116-01
Title	APSCT
Number of Layers	8
Size of the PCB	292 X 366.66 (mm) +/- 0.1 mm
Placement components	SMD Top/Bottom, Through-hole Top/Bottom
Number of signal layers	4
Number of plane layers	4
Number of Non-signal layers	2 (mask)
Silkscreen	top and bottom (user layer)
Number of Pins	3685
Number of Nets	667
Number of Components	925
Number of Vias	3618
Vias filling	2605 Yes, via in pad is used. Holes < 0.4mm are filled and capped.
Total number of Trough Holes	4441
Smallest hole diameter	0.3 mm Through Hole (finished size)
Smallest route size	0.13 mm
Smallest Isolation / clearance	0.15 mm
PCB material and type	ISOLA FR408HR
Material thickness	Total 2.4 mm
Copper thickness	See master drawing.
Etch Tolerance	10%
Via Plating	Through and Buried: >20um
Finishing	Gold (ENIG)
Impedance trace on layer	See section appendix
Hole tolerances	Press fit connectors are placed on the board, see drill drawing for hole tolerances.
Reports	All reports showing correct production have to be delivered. This includes impedances, layer and copper thickness and electrical test reports. See Master Drawing notes pag. 6 (not in yet)
PCB Testing	Electrical test (open circuit/short circuit)



This publication is part of the project DUPLLO (with project number 175.2017.012 of the research program "Investeren in NWO-groot" which is (partly) financed by the Dutch Research Council (NWO).

PSF00167
3.0
11-03-2022

4 List of Files

ODB++	apsct_180222.tgz
Statistics	On request

5 Filled & capped via

The via's should be filled according **IPC4761 TYPE VII** via (filled and capped via), see Figure 2

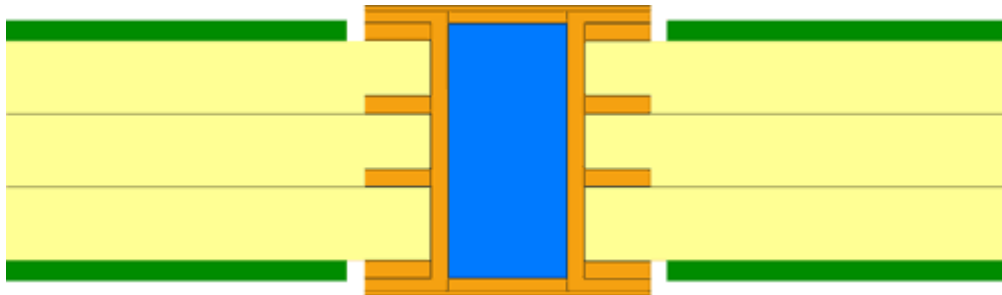


Figure 1 Filled and capped via

6 General

For technical information contact can be made with;

Designer: *Gijs Schoonderbeek (ASTRON)*
 Phone; (+31) (0)521 595 110
 E-mail; schoonderbeek@astron.nl

NOTES:

PCB Specifications

- [1] Fabricate boards in accordance with IPC6011 / IPC6012 CLASS
- [2] Finished boards must meet quality and conformance testing and inspection as specified
- [3] Drill boards using drill data, drill pattern and hole schedule.
Hole locations may vary within 0.125mm max. about true position.
- [4] All holes are plated through unless noted otherwise.
Minimum copper plating in plated holes to be 25um.
Maximum copper plating in plated holes to be 50um.
- [5] Plating primary and secondary side: ENIG
- [6] Minimum annular ring:
internal: 20um
external: 25um
- [7] Bow and twist shall not exceed 0.75% measured in accordance with IPC-TM Method 2.4.22.
- [8] All via's with < 0.35mm holes shall be filled and capped
- [9] Differential pair impedance tolerance less than 10%
- [10] Construction to be soldermask over bare copper (SM0BC)
Apply to primary and secondary sides in accordance with IPC-SM-840 (Class T).
- [11] Soldermask thickness 5um min. / 30um maximal.
- [12] Soldermask to be light green in color and transparent.
- [13] PCB Repairs: Repairs of damaged traces is not permitted.
- [14] Non-Functional pads can be removed.

Testing

- [15] All bare boards shall be electrically tested using CAD generated netlist data.
Electrical testing shall follow the guidelines established by IPC-ET-652.
Guidelines and requirements for electrical testing of unpopulated printed boards.
- [16] Each production panel shall pass a thermal test in accordance IPC-TM-650 Method 2.6.27 for a reflow temperature of 260 deg C.
- [17] For each production batch the line impedance of controlled impedance lines (100 Ohm and or 50 Ohm) on all impedance layers shall be tested in accordance IPC-TM-650 Method 2.5.5.7.

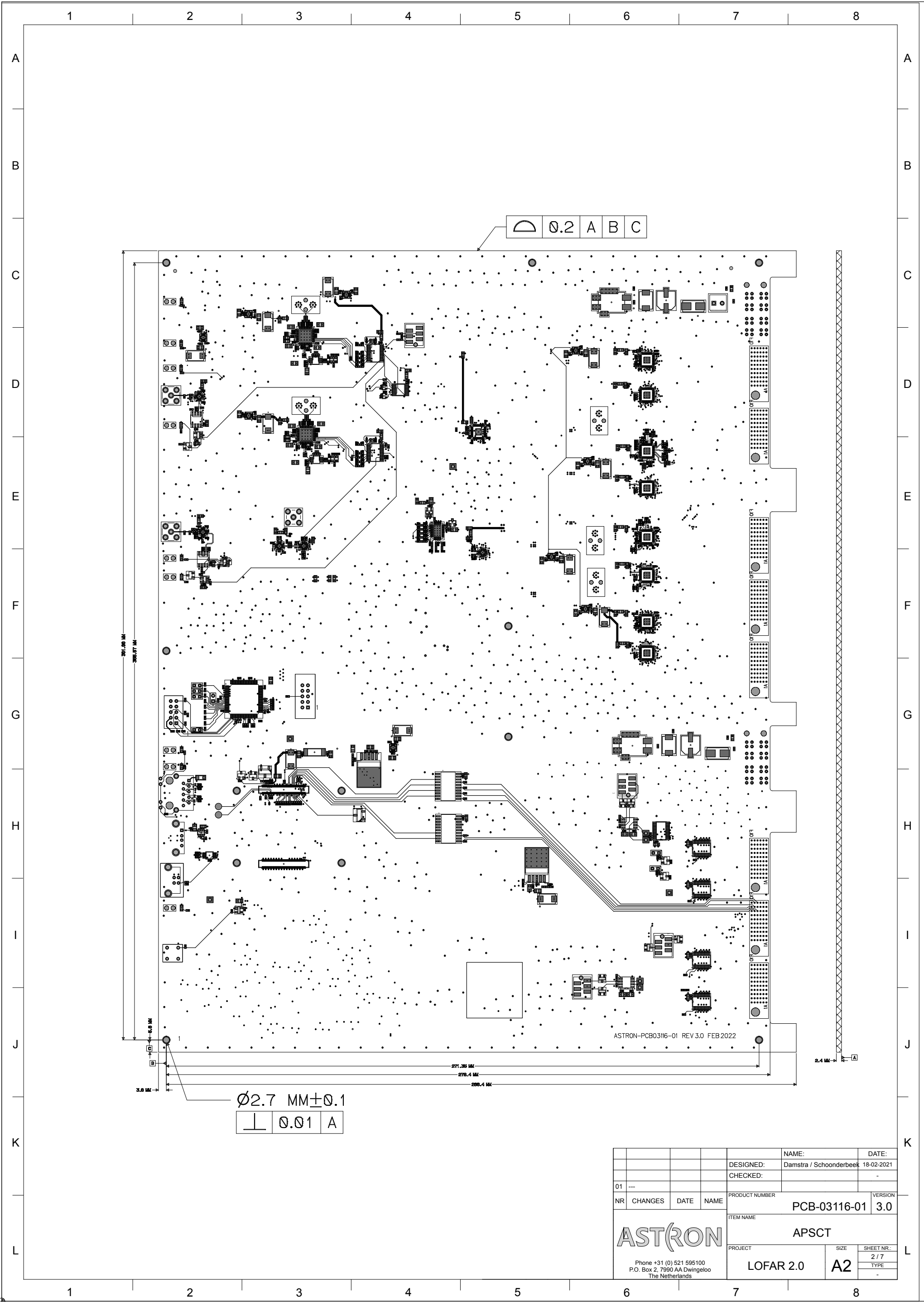
Other

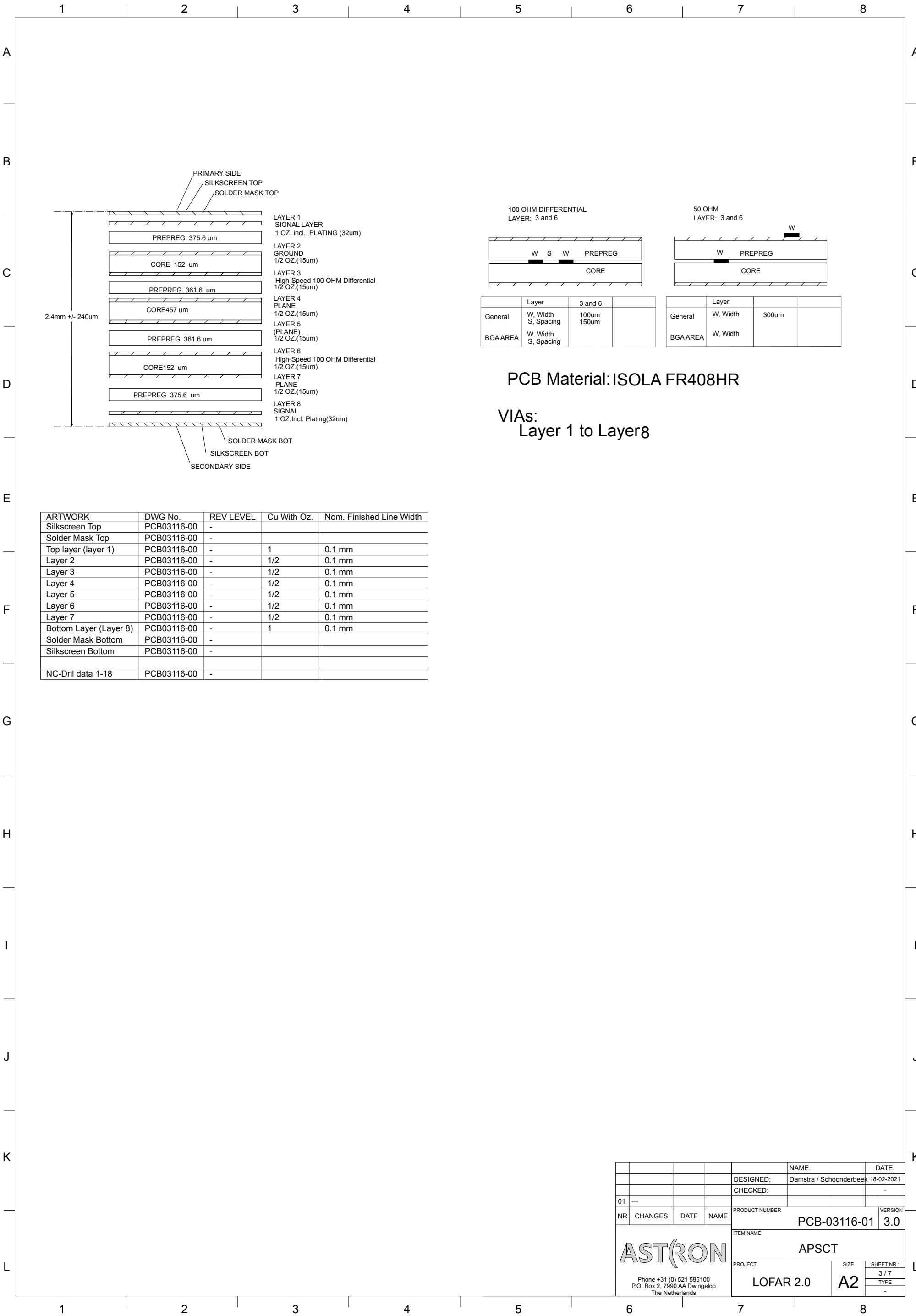
- [18] Board fabricator shall apply serial number, date code and UL Marking at the indicated location on the primary side.

Assembly Specifications

- [19] All boards shall be assembled according IPC-A-612 Class 2 specification for Type 2 Class 2 boards

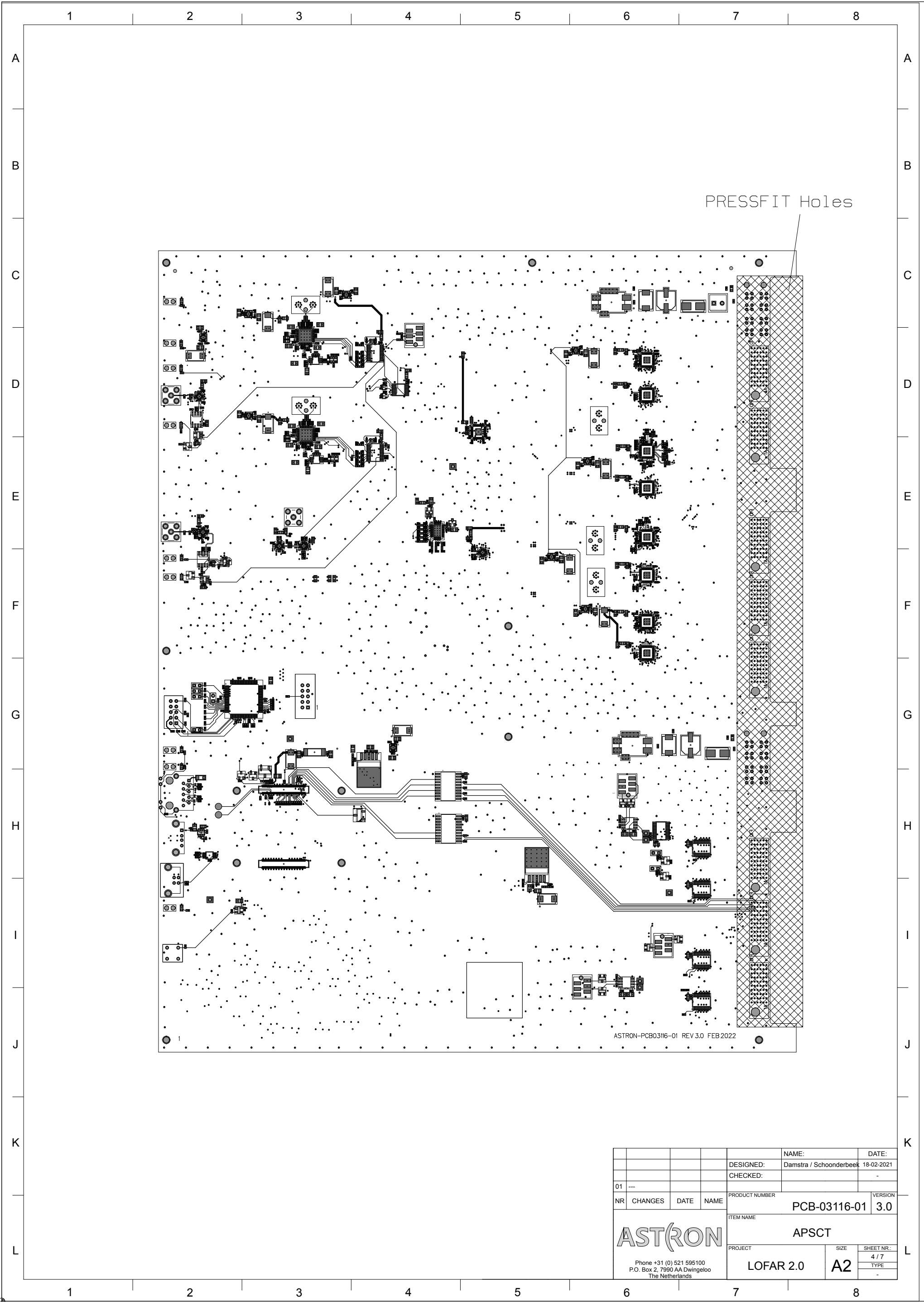
					NAME:	DATE:
				DESIGNED:	Damstra / Schoonderbeek	18-02-2021
				CHECKED:		-
01	---					
NR	CHANGES	DATE	NAME	PRODUCT NUMBER	PCB-03116-01	VERSION 3.0
ASTRON Phone +31 (0) 521 595100 P.O. Box 2, 7990 AA Dwingeloo The Netherlands				ITEM NAME		
				APSCT		
				PROJECT	LOFAR 2.0	SIZE A2
						SHEET NR.: 1 / 7 TYPE -





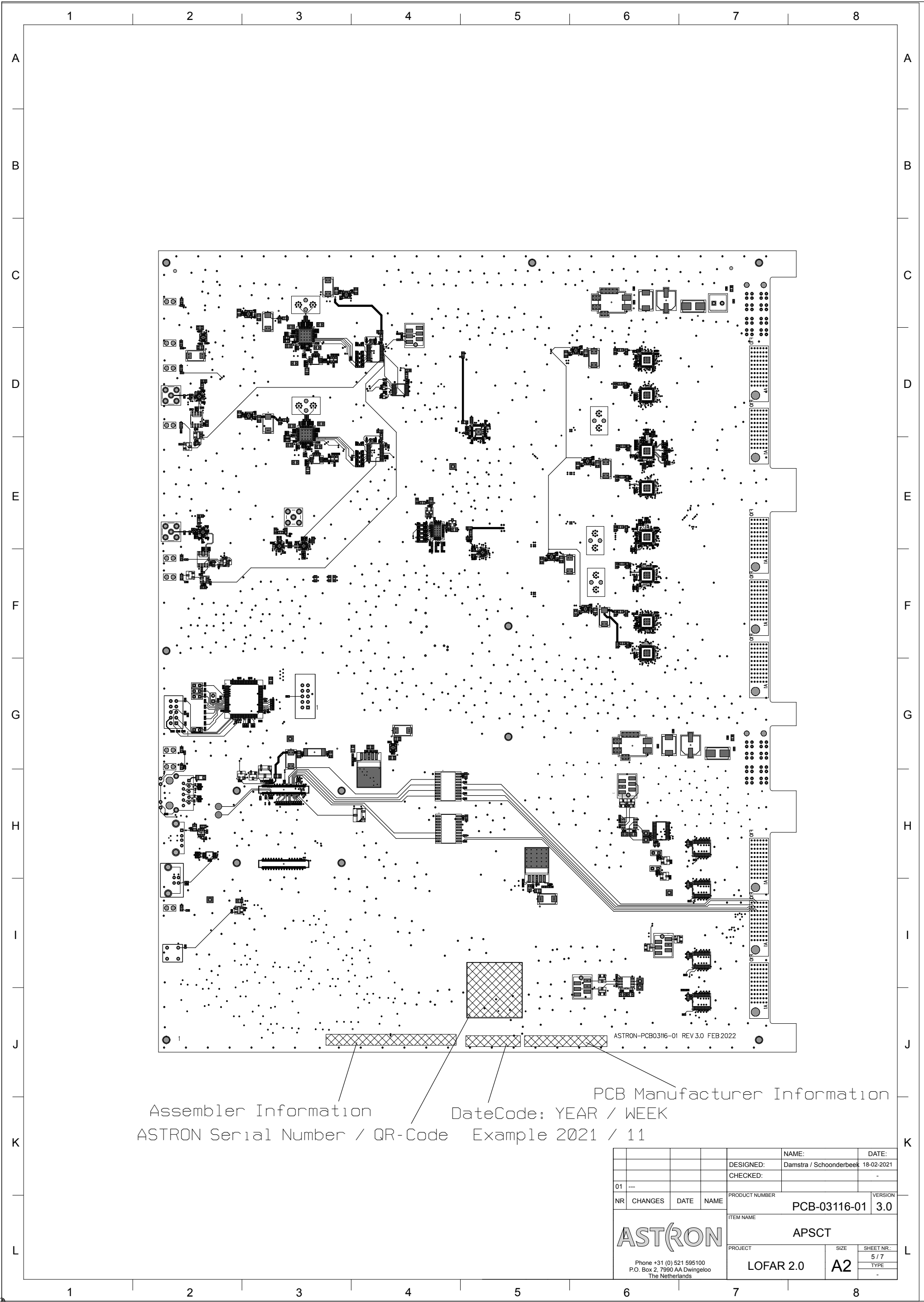
ARTWORK	DWG No.	REV LEVEL	Cu With Oz.	Nom. Finished Line Width
Silkscreen Top	PCB03116-00	-		
Solder Mask Top	PCB03116-00	-		
Top layer (layer 1)	PCB03116-00	-	1	0.1 mm
Layer 2	PCB03116-00	-	1/2	0.1 mm
Layer 3	PCB03116-00	-	1/2	0.1 mm
Layer 4	PCB03116-00	-	1/2	0.1 mm
Layer 5	PCB03116-00	-	1/2	0.1 mm
Layer 6	PCB03116-00	-	1/2	0.1 mm
Layer 7	PCB03116-00	-	1/2	0.1 mm
Bottom Layer (Layer 8)	PCB03116-00	-	1	0.1 mm
Solder Mask Bottom	PCB03116-00	-		
Silkscreen Bottom	PCB03116-00	-		
NC-Drill data 1-18	PCB03116-00	-		

					NAME:	DATE:
					DESIGNED:	Damstra / Schoonderbeek 18-02-2021
					CHECKED:	-
01	---					
NR	CHANGES	DATE	NAME	PRODUCT NUMBER	PCB-03116-01	VERSION 3.0
ASTRON Phone +31 (0) 521 595100 P.O. Box 2, 7990 AA Dwingeloo The Netherlands				ITEM NAME		
				APSCT		
				PROJECT	LOFAR 2.0	SIZE A2
						SHEET NR.: 3 / 7 TYPE -



ASTRON-PCB03116-01 REV 3.0 FEB 2022

				NAME:		DATE:	
				DESIGNED:		Damstra / Schoonderbeek	
				CHECKED:		-	
01	---						
NR	CHANGES	DATE	NAME	PRODUCT NUMBER			VERSION
				PCB-03116-01			3.0
ASTRON Phone +31 (0) 521 595100 P.O. Box 2, 7990 AA Dwingeloo The Netherlands				ITEM NAME			
				APSCT			
				PROJECT		SIZE	SHEET NR.:
				LOFAR 2.0		A2	4 / 7
						TYPE	
						-	

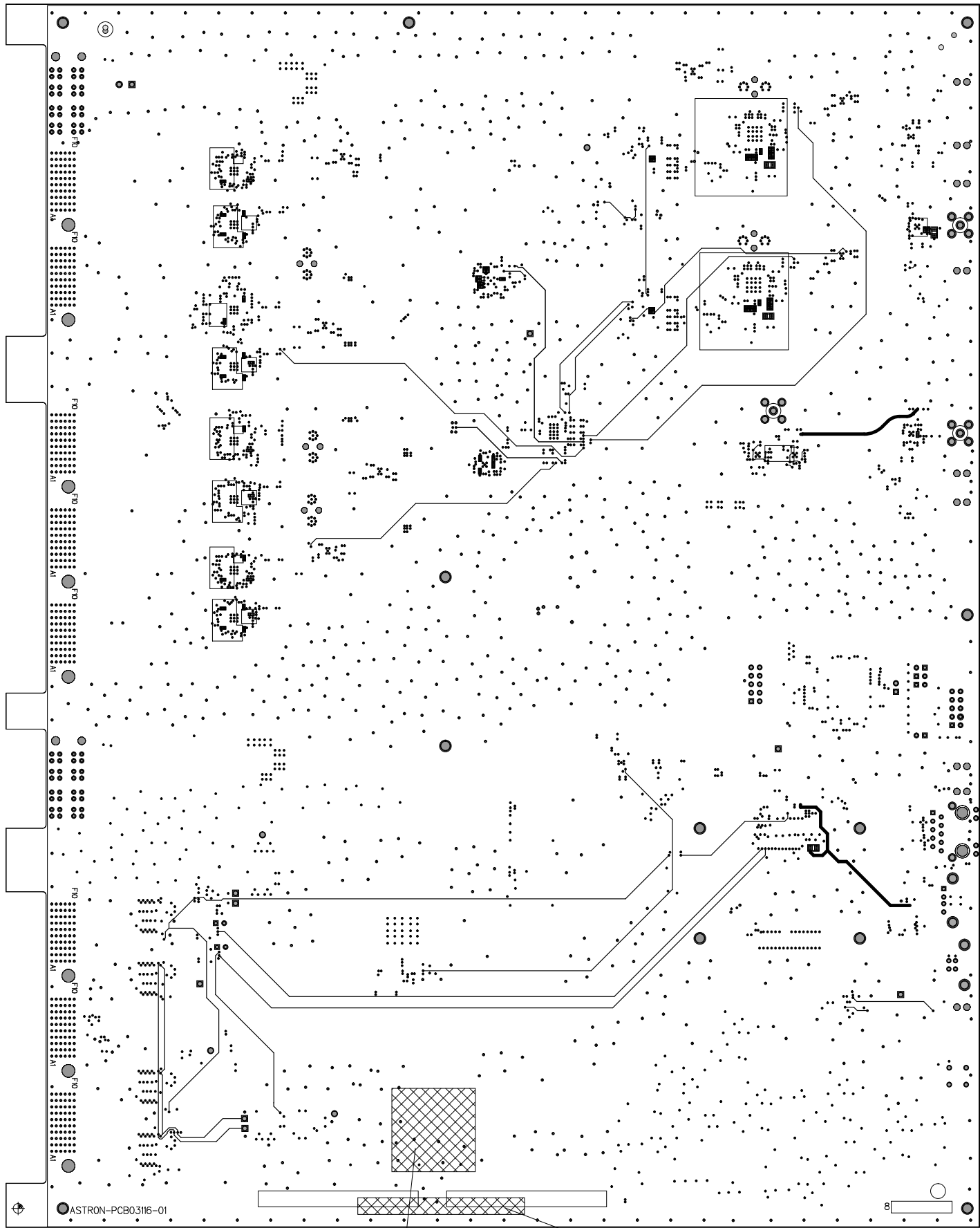


Assembler Information
ASTRON Serial Number / QR-Code

DateCode: YEAR / WEEK
Example 2021 / 11

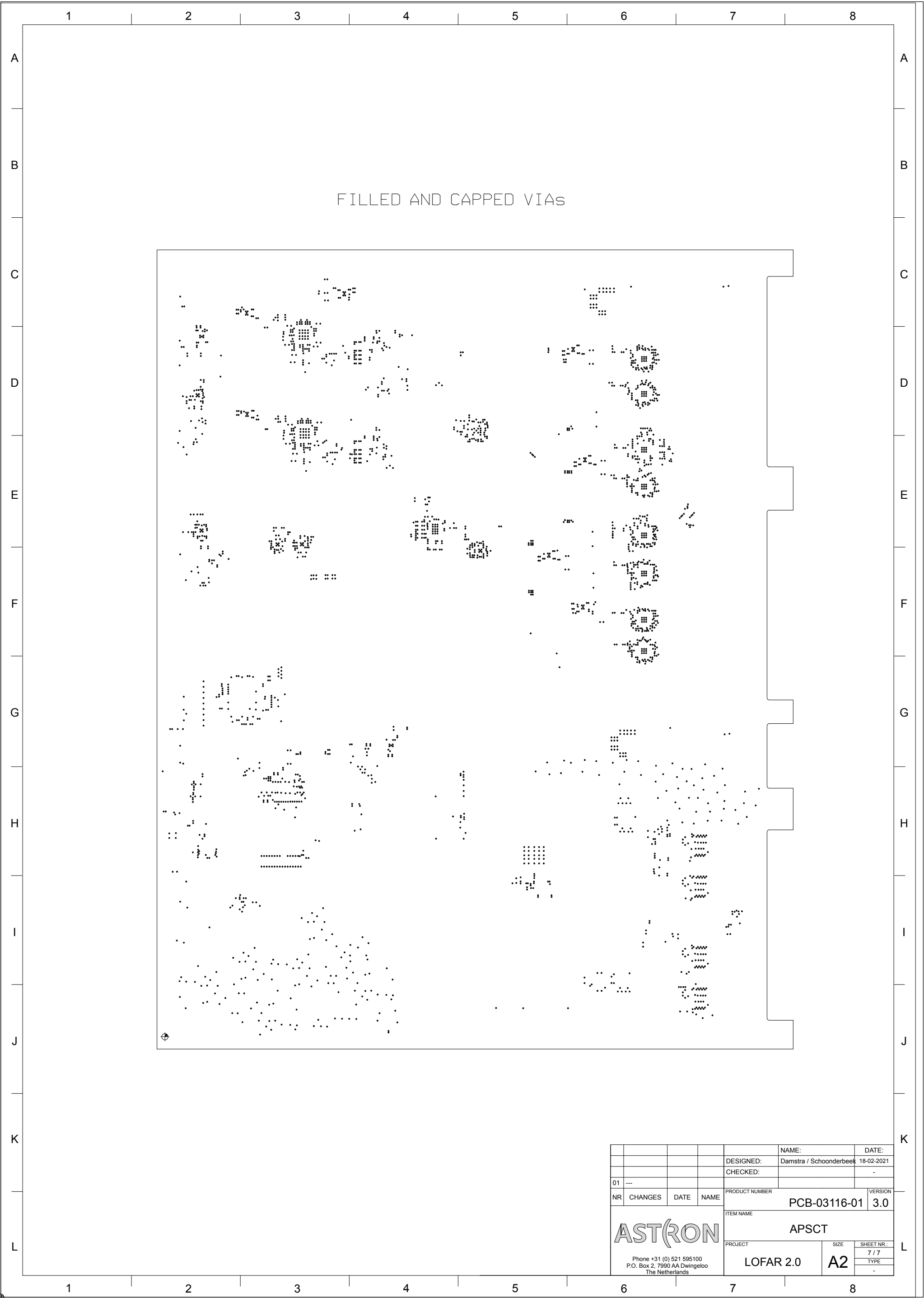
PCB Manufacturer Information

				NAME:	DATE:
				DESIGNED:	Damstra / Schoonderbeek 18-02-2021
				CHECKED:	-
01	---				
NR	CHANGES	DATE	NAME	PRODUCT NUMBER	VERSION
				PCB-03116-01	3.0
ASTRON Phone +31 (0) 521 595100 P.O. Box 2, 7990 AA Dwingeloo The Netherlands				ITEM NAME	
				APSCT	
				PROJECT	SIZE
				LOFAR 2.0	A2
					SHEET NR.: 5 / 7
					TYPE -



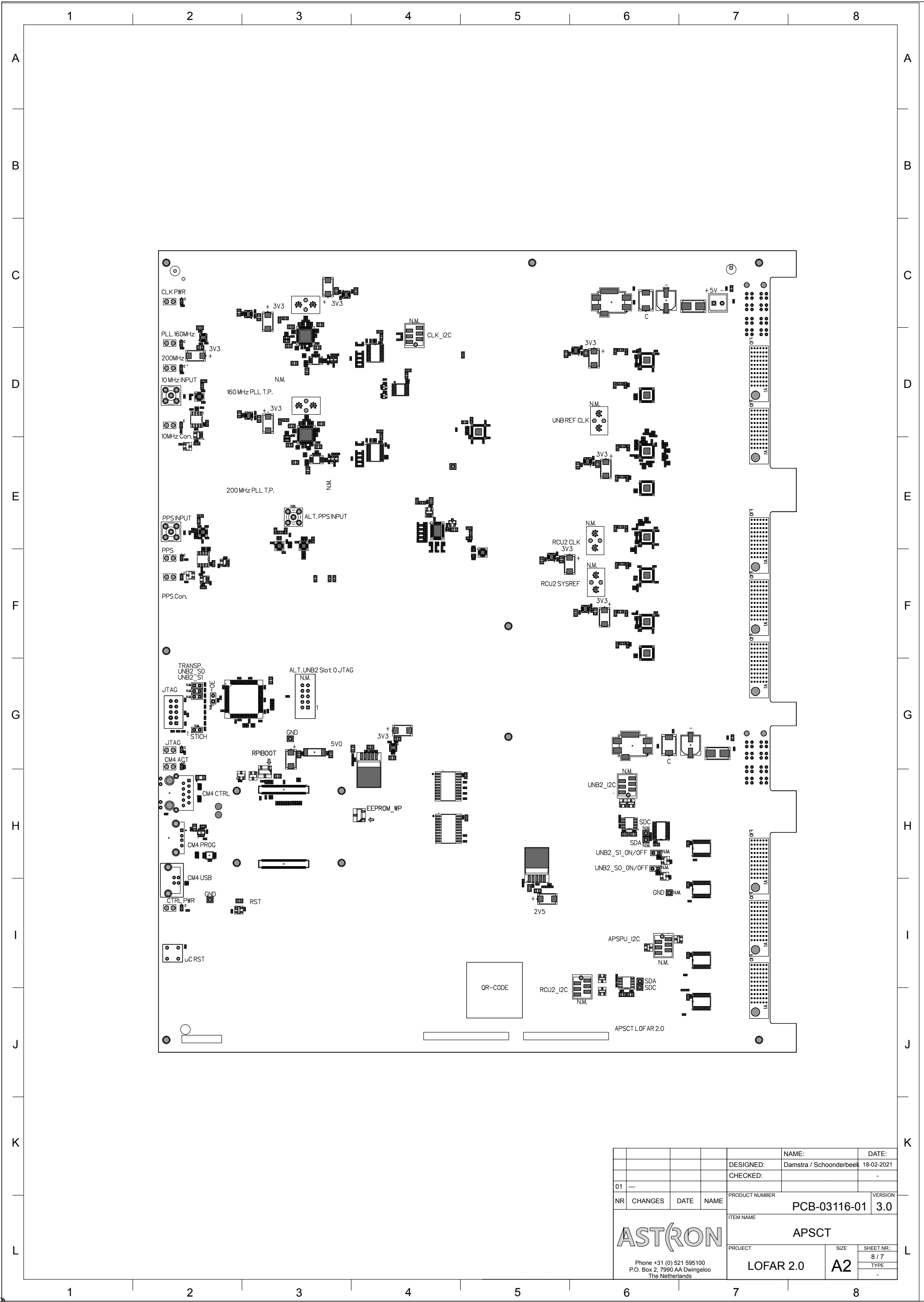
PCB Manufacturer Information

OPTIONAL Assembly Manufacturer Information



FILLED AND CAPPED VIAs

					NAME:	DATE:
				DESIGNED:	Damstra / Schoonderbeek	18-02-2021
				CHECKED:		-
01	---					
NR	CHANGES	DATE	NAME	PRODUCT NUMBER	PCB-03116-01	VERSION 3.0
ASTRON Phone +31 (0) 521 595100 P.O. Box 2, 7990 AA Dwingeloo The Netherlands				ITEM NAME	APSCT	
PROJECT					SIZE	SHEET NR.:
LOFAR 2.0					A2	7 / 7
						TYPE
						-



				NAME:		DATE:	
				DESIGNED:		Damstra / Schoonderbeek	
				CHECKED:		-	
01	---						
NR	CHANGES	DATE	NAME	PRODUCT NUMBER			VERSION
				PCB-03116-01			3.0
ASTRON Phone +31 (0) 521 595100 P.O. Box 2, 7990 AA Dwingeloo The Netherlands				ITEM NAME			
				APSCT			
				PROJECT		SIZE	SHEET NR.:
				LOFAR 2.0		A2	8 / 7
						TYPE	
						-	